

Applicant : Hongxin Song et al.  
Serial No. : 10/600,419  
Filed : June 20, 2003  
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Attorney's Docket No.: MP0275 / 13361-045001

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**REMARKS**

Claims 1-75 are pending, with claims 1, 12, 22, 34, 45, 53 and 64 being independent.

Claims 22-52 and 64-75 are allowed. Reconsideration and allowance of the above-referenced application are respectfully requested.

**Allowed Subject Matter:**

The indication that claims 22-52 and 64-75 are allowed is acknowledged and appreciated. The claims are retained. Moreover, it is agreed that the features recited in the Examiner's statement of reasons for allowance are not taught or suggested by the art of record, and that some or all of the allowed independent claims 22, 34, 45 and 64 are distinguished from the art of record for at least the reasons stated by the Examiner. Applicant does not concede that the stated reasons are the only grounds for patentability of the allowed claims, that the claim limitations excluded from the reasons for allowance are taught or suggested by the art of record, or that all of the limitations are necessary for patentability of the allowed claims or other claims directed to the disclosed subject matter. Additionally, each allowed claim stands on its own.

**Rejections under 35 U.S.C. § 102(b):**

Claims 1-21 and 53-63 stand rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by U.S. Patent No. 6,009,549 to Bliss et al. (hereinafter, Bliss). This contention is respectfully traversed.

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Bliss describes a disk storage system in which the "estimated binary sequence output by the sequence detector is buffered in a data buffer to facilitate the error detection and correction process, and to allow for retroactive and split-segment symbol synchronization." (See *Bliss* at Abstract and col. 4, lines 25-28.) Bliss, as best understood, describes using a raw samples buffer to store read signal samples, and adjusting "read channel parameters" during each pass over the samples stored in the samples buffer. (See *Bliss* at col. 15, line 56 to col. 16, line 22.) Moreover, in an alternative embodiment,

all of the samples stored in the samples buffer 104 are processed to compute an "average" optimal setting for all of the loop filters. In this manner, the loop filters can operate statically using the computed average or optimal value while reprocessing the samples during the retry operation.

(See *Bliss* at col. 16, lines 23-28.) This use of an "average" optimal setting for the loop filters does not anticipate the presently claimed subject matter.

Independent claim 1 recites, "an input to receive a signal; a buffer responsive to the input to store the signal; a detector responsive to the input to interpret the signal as discrete values; and an averaging circuit responsive to the buffer and the detector to cause interpretation, by the detector during a retry mode, of a new signal comprising an average of a previous signal stored in the buffer and a current signal." (Emphasis added.) The cited portion of Bliss does not describe circuitry to process a new signal comprising an average of a previous signal stored in the buffer and a current signal during a retry mode. In fact, Bliss teaches away from this idea by clearly stating that the preferred data buffer size is large enough to avoid rereading the data

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sector from disk during a retry mode. (*See Bliss* at col. 15, lines 59-64.) *Bliss* never suggests reading the same disk portion twice, to obtain two sets of data samples for the same data, and averaging the two sets of data samples for processing in a retry mode. The averaging performed in *Bliss*, as best understood by Applicant, involves processing all stored samples to compute an average optimal setting for all the loop filters. Thus, *Bliss* does not anticipate independent claim 1, and this claim should be in condition for allowance.

Independent claim 12 recites, “a storage medium; a head assembly operable to generate a read signal from the storage medium; a buffer that saves the read signal generated by the head assembly; a detector that interprets the read signal as discrete values; an averaging circuit responsive to the buffer and the detector; and a control circuit responsive to the averaging circuit to cause interpretation by the detector in a retry mode of a new read signal comprising an average of a previous read signal stored in the buffer and a current read signal.” (Emphasis added.) Thus, independent claim 12 should be allowable for at least the same reasons set forth above with respect to claim 1.

Independent claim 53 recites, “means for receiving a signal; means for storing the signal; means for interpreting the signal as discrete values; and retry-mode means for interpreting a new signal comprising an average of a stored signal and a current signal.” (Emphasis added.) Thus, independent claim 53 should be allowable for at least the same reasons set forth above with respect to claim 1.

Dependent claims 2-11, 13-21, and 54-63 should be allowable at least due to their respective base claims and the additional recitations they contain.

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Conclusion

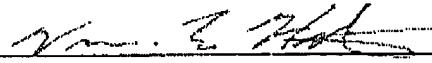
The foregoing comments made with respect to the positions taken by the Examiner are not to be construed as acquiescence with other positions of the Examiner that have not been explicitly contested. Accordingly, the arguments for patentability of a claim should not be construed as implying that there are not other valid reasons for patentability of that claim or other claims.

In view of the remarks herein, claims 1-75 should be in condition for allowance. A formal notice of allowance is respectfully requested.

Please apply any necessary charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: September 27, 2006

  
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